Summary of Pricing Schedules

Target Group	Description	Price ($K)
4.0	**SST High-Level Technical Requirements**	**$ -**
4.1	**SST Hardware High-Level Requirements**	**$ -**
4.1.1	Scalable Cluster of SMPs	$ -
4.1.1.1	Sustained Stewardship TeraFLOP SMP Scalable Cluster (MR)	$ -
4.1.1.2	SST Component Scaling (MR)	$ -
4.1.1.2.1	Additional Intra-Cluster Network Bi-Section Bandwidth (TR)	$ -
4.1.1.3	SST Applications Memory (MO)	$ -
4.1.1.4	Cluster Wide High Resolution Event Sequencing (TR)	$ -
4.1.1.5	Cluster Interconnect Reliability and Performance (TR)	$ -
4.1.1.6	Cluster Interconnect Link Bandwidth (TR)	$ -
4.1.1.7	Cluster Interconnect Latency (TR)	$ -
4.1.1.8	Remote Memory Access (TR)	$ -
4.1.2	Shared Memory Multi-Processor	$ -
4.1.2.1	SMP Platform (MR)	$ -
4.1.2.2	CPU Characteristics (MR)	$ -
4.1.2.3	Minimum CPU Performance (TR)	$ -
4.1.2.4	Minimum SMP Performance (TR)	$ -
4.1.2.5	IEEE 754 32-Bit Floating Point Numbers (TR)	$ -
4.1.2.6	Test-And-Set Instruction (TR)	$ -
4.1.2.7	Programmable Clock (TR)	$ -
4.1.2.8	Hardware Interrupt (TR)	$ -
4.1.2.9	Hardware Performance Monitors (TR)	$ -
4.1.2.10	Hardware Debugging Support (TR)	$ -
4.1.3	Memory Hierarchy	$ -
4.1.3.1	Shared Main Memory (MR)	$ -
4.1.3.2	Memory Hierarchy Latency (TR)	$ -
4.1.3.3	Additional Physical Address Space (TR)	$ -
4.1.3.4	Memory Consistency Model (TR)	$ -
4.1.4	RED/BLACK Resource Usage Model	$ -
4.1.4.1	RED/BLACK Code Development Environments (MO)	$ -
4.1.4.2	RED/BLACK I/O Resources (MR)	$ -
4.1.4.3	RED/BLACK Migration (MR)	$ -
4.1.4.4	SST RAID Arrays (TR)	$ -

Summary of Pricing Schedules

Target Group	Description	Price ($K)
4.1.4.5	Single Sustained I/O Bandwidth (TR)	$ -
4.1.4.6	Parallel Sustained I/O Bandwidth (TR)	$ -
4.1.4.7	Cluster High Speed External Network Interfaces (TR)	$ -
4.1.4.8	Cluster I/O Upgradeability (TR)	$ -
4.1.5	Reliability, Availability, Serviceability and Maintenance	$ -
4.1.5.1	Power Cycling (TR)	$ -
4.1.5.2	Hot Swap Capability (TR)	$ -
4.1.5.3	Production Level System Stability (TR)	$ -
4.1.5.4	System Down Time (TR)	$ -
4.1.5.5	FRU Diagnostics (TR)	$ -
4.1.5.6	Failure Isolation Mode (TR)	$ -
4.1.5.7	Scalable System Diagnostics (TR)	$ -
4.1.5.8	System Graceful Degradation Failure Mode (TR)	$ -
4.1.5.9	SMP Processor Failure Tolerance (TR)	$ -
4.1.5.10	SMP Memory Failure Tolerance (TR)	$ -
4.1.5.11	Replacement Parts and Maintenance (MR)	$ -
4.2	**SST Software High-Level Requirements**	**$ -**
4.2.1	Operating System	$ -
4.2.1.1	SMP Base Operating System and License (MR)	$ -
4.2.1.1.1	X/Open OS Compliance (TR)	$ -
4.2.1.1.2	Single System Image (TR)	$ -
4.2.1.1.3	Thread Packages (TR)	$ -
4.2.1.1.4	System Utilities (TR)	$ -
4.2.1.1.5	Job Checkpointing (TR)	$ -
4.2.1.2	Cluster Wide Fault Tolerance and Graceful Degradation of Service (TR)	$ -
4.2.1.3	Networking Protocols (MR)	$ -
4.2.1.4	Third Party Transfer Support (TR)	$ -
4.2.1.5	Group Routing (MR)	$ -
4.2.1.6	File Systems (TR)	$ -
4.2.2	Distributed Computing Middleware	$ -
4.2.2.1	OSF DCE (MR)	$ -
4.2.2.1.1	Distributed File System Server (MR)	$ -
4.2.2.1.2	Cluster Wide Service Security (MR)	$ -
4.2.2.1.3	Transarc Encina (MR)	$ -

Summary of Pricing Schedules

Target Group	Description	Price ($K)
4.2.2.2	Object Request Broker (TR)	$ -
4.2.3	Cluster Wide Resource Management and Accounting	$ -
4.2.3.1	Cluster Wide Resource Management (TR)	$ -
4.2.3.1.1	Cluster Wide Resource Limits (TR)	$ -
4.2.3.1.2	Cluster Wide Resource Management API (TR)	$ -
4.2.3.2	Cluster Wide Job Accounting (TR)	$ -
4.2.3.3	Accounting for System (Root) Usage (TR)	$ -
4.2.3.4	Cluster Wide Job Management (MR)	$ -
4.2.3.5	Cluster Wide Job Scheduling (MR)	$ -
4.2.3.5.1	Cluster and SMP Gang Scheduling (TR)	$ -
4.2.3.5.2	Cluster Wide Job Scheduling Interface (TR)	$ -
4.2.4	Cluster System Administration Tools	$ -
4.2.4.1	Single Point for Cluster System Administration (MR)	$ -
4.2.4.2	Cluster System Debugging and Performance Analysis (TR)	$ -
4.2.4.3	Centralized Repository (TR)	$ -
4.2.4.4	User Maintenance (TR)	$ -
4.2.5	Parallelizing Compilers/Translators	$ -
4.2.5.1	Baseline Languages (MR)	$ -
4.2.5.1.1	Common Preprocessor for Baseline Languages (TR)	$ -
4.2.5.1.2	Base Language Interprocedural Analysis (TR)	$ -
4.2.5.1.3	Baseline Language Compiler Generated Listings (TR)	$ -
4.2.5.1.4	C++ Functionality (TR)	$ -
4.2.5.1.5	Cray Pointer Functionality (TR)	$ -
4.2.5.2	High Performance Fortran (TR)	$ -
4.2.6	Debugging and Tuning Tools	$ -
4.2.6.1	Debugger for Cluster Wide Applications (MR)	$ -
4.2.6.1.1	Visual Representation of Data (TR)	$ -
4.2.6.1.2	Fast Conditional Data Watchpoints and Breakpoints (TR)	$ -
4.2.6.1.3	Memory Leak Debugging (TR)	$ -
4.2.6.1.4	Debugging Optimized Applications (TR)	$ -
4.2.6.1.5	Debugger Expression Evaluator (TR)	$ -
4.2.6.1.6	Parallel Debugger Barrier-Points (TR)	$ -
4.2.6.1.7	Post-Mortem Debugging (TR)	$ -
4.2.6.1.8	Symbol Table (TR)	$ -

Summary of Pricing Schedules

Target Group	Description	Price ($K)
4.2.6.1.9	Data Aggregation (TR)	$ -
4.2.6.2	Stack Traceback (TR)	$ -
4.2.6.3	Lightweight Corefile API (TR)	$ -
4.2.6.4	Profiling Tools for Cluster Applications (MR)	$ -
4.2.6.5	Event Tracing Tools for Cluster Applications (MR)	$ -
4.2.6.5.1	Message-Passing Event Tracing (TR)	$ -
4.2.6.6	Performance Statistics Tools for Cluster Applications (MR)	$ -
4.2.6.7	Cluster Wide Application Development Tool API (TR)	$ -
4.2.6.8	Cluster Wide Application Development Tool GUI (MR)	$ -
4.2.6.9	Timer API (TR)	$ -
4.2.7	Applications Building	$ -
4.2.7.1	Linker and Library Building Utility (MR)	$ -
4.2.7.2	Make Utility (MR)	$ -
4.2.7.3	Parallel Make (TR)	$ -
4.2.7.4	Source Code Management (TR)	$ -
4.2.7.5	Dynamic Processor Allocation (TR)	$ -
4.2.8	Application Programming Interfaces	$ -
4.2.8.1	Optimized Message-Passing Interface (MPI) Library (MR)	$ -
4.2.8.2	MPI2 Library.(TR)	$ -
4.2.8.3	Visual Display of Message Traffic.(TR)	$ -
4.2.8.4	Optimized Parallel Virtual Machine (PVM) Library.(TR)	$ -
4.2.8.5	Parallel I/O API (TR)	$ -
4.2.8.5.1	Parallel I/O Buffer Attributes (TR)	$ -
4.2.8.5.2	Parallel I/O Sequential Write (TR)	$ -
4.2.8.5.3	Asynchronous Parallel I/O (TR)	$ -
4.2.8.5.4	High-Level Parallel I/O API (TR)	$ -
4.2.8.6	Graphical User Interface API (MR)	$ -
4.2.8.7	Visualization API (TR)	$ -
4.2.8.8	Math Libraries (TR)	$ -
4.2.9	Operating System Security (TR)	$ -
4.2.9.1	Login Information (TR)	$ -
4.2.9.2	Audit Capability (MR)	$ -
4.2.10	Compliance with DOE Security Mandates (MR)	$ -
4.2.11	Cluster Environment On-Line Document (TR)	$ -

Summary of Pricing Schedules

Target Group	Description	Price ($K)
4.2.12	SST Applications Development Support (MR)	$ -
5.0	**ID High-Level Technical Requirements**	**$ -**
5.1	**Initial Delivery Hardware Requirements**	**$ -**
5.1.1	Hierarchical Hardware Model	$ -
5.1.1.1	ID SMP Scalable Cluster (MR)	$ -
5.1.1.2	CPU Performance Model (TR)	$ -
5.1.1.3	Hierarchical Memory Model (TR)	$ -
5.1.1.4	Message Passing Model (TR)	$ -
5.1.1.5	Parallel I/O Model (TR)	$ -
5.1.2	ID Performance Characteristics	$ -
5.1.2.1	ID Single CPU Performance (TR)	$ -
5.1.2.2	ID SMP Cluster Performance (MR)	$ -
5.1.2.3	ID System Component Scaling (TR)	$ -
5.1.2.4	ID SMP Cluster Message Passing Performance (TR)	$ -
5.1.2.5	Sustained ID Serial and Parallel I/O Performance (TR)	$ -
5.1.2.6	ID SMP Cluster External Networking (TR)	$ -
5.1.3	RED/BLACK Resource Usage Model	$ -
5.1.3.1	RED/BLACK Partitions (MR)	$ -
5.1.3.1.1	RED/BLACK Resource Split (MO)	$ -
5.1.3.1.2	RED/BLACK Partition Switching (MO)	$ -
5.1.3.2	ID RAID Arrays (TR)	$ -
5.1.3.3	Cluster I/O Upgradeability (TR)	$ -
5.1.4	Reliability, Availability, Serviceability and Maintenance (TR)	$ -
5.1.4.1	Replacement Parts and Maintenance (MR)	$ -
5.2	**Initial Delivery Software Requirements**	**$ -**
5.2.1	Operating System	$ -
5.2.1.1	SMP Base Operating System and License (MR)	$ -
5.2.1.2	Networking Protocols (MR)	$ -
5.2.1.3	Third Party Transfers (TR)	$ -
5.2.1.4	Group Routing (MR)	$ -
5.2.2	Distributed Computing Environment (MR)	$ -
5.2.2.1	Distributed File System Server (MR)	$ -

Summary of Pricing Schedules

Target Group	Description	Price ($K)
5.2.2.2	Transarc Encina (MR)	$ -
5.2.3	Cluster Wide Resource Management and Accounting (TR)	$ -
5.2.4	Cluster System Administration Tools (TR)	$ -
5.2.5	Parallelizing Compilers/Translators	$ -
5.2.5.1	Baseline Languages (MR)	$ -
5.2.5.1.1	Cray Pointer Functionality (TR)	$ -
5.2.5.2	Hierarchical Programming Model (TR)	$ -
5.2.6	Debugging and Tuning Tools	$ -
5.2.6.1	Debugger for Parallel Applications (MR)	$ -
5.2.7	Applications Building	$ -
5.2.7.1	Linker and Library Building Utility (MR)	$ -
5.2.7.2	Make Utility (MR)	$ -
5.2.8	Application Programming Interfaces	$ -
5.2.8.1	Optimized Message-Passing Interface (MPI) Library (MR)	$ -
5.2.8.2	Optimized Parallel Virtual Machine (PVM) Library (TR)	$ -
5.2.8.3	Parallel I/O API (TR)	$ -
5.2.8.3.1	Parallel I/O Buffer Attributes (TR)	$ -
5.2.8.3.2	Parallel I/O Sequential Write (TR)	$ -
5.2.8.3.3	High-Level Parallel I/O API (TR)	$ -
5.2.8.4	Graphical User Interface API (MR)	$ -
5.2.8.5	Math Libraries (TR)	$ -
5.2.9	SST Software Environment Features for ID (TR)	$ -
5.2.10	Compliance with DOE Security Mandates (MR)	$ -
5.2.11	Cluster Environment On-Line Documentation (TR)	$ -
5.2.12	ID Applications Development Support (MR)	$ -
6.0	**Implementing a Sustained Stewardship TeraFLOP**	**$ -**
6.1	**Detailed Project Plan**	**$ -**
6.1.1	Detailed Project Management Plan (MR)	$ -
6.1.2	Detailed Hardware Project Plan (MR)	$ -
6.1.3	Detailed Software Project Plan (MR)	$ -
6.2	**Project Milestones**	**$ -**

Summary of Pricing Schedules

Target Group	Description	Price ($K)
6.2.1	Detailed Project Plan (MR)	$ -
6.2.2	Initial Delivery (ID) System (MR)	$ -
6.2.3	Second Initial Delivery (ID) System (MO)	$ -
6.2.4	ID Applications Development Support (MR)	$ -
6.2.5	FY97 Plan and Review (MR)	$ -
6.2.6	Technology Refresh (TR)	$ -
6.2.7	FY98 Plan and Review (MR)	$ -
6.2.8	SST Applications Development Support (MR)	$ -
6.2.9	Scalable Development Environment Demonstration (TR)	$ -
6.2.10	Sustained Stewardship TeraFLOP (SST) Demonstration (TR)	$ -
6.2.11	Scalable Development Environment Demonstration (MR)	$ -
6.2.12	Sustained Stewardship TeraFLOP (SST) Demonstration (MR)	$ -
6.2.13	SST Installation (MR)	$ -
6.2.14	FY99 Plan and Review (MR)	$ -
6.2.15	Memory Installation (MO)	$ -
6.3	**Performance Reviews (MR)**	**$ -**
	Vendor-Proposed Options	**$ -**
	Option 1	$ -
	Option 2	$ -
	Option 3	$ -
	Option 4	$ -
	Option 5	$ -

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